IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

STMICROELECTRONICS, INC., Plaintiff, v. SANDISK CORP., Defendant, Counterclaim Plaintiff, v. STMICROELECTRONICS, N.V., and STMICROELECTRONICS, INC. Counterclaim Defendants.	C.A. NO. 4:05CV45 Judge Michael H. Schneider Magistrate Judge Donald D. Bush Jury Trial Demanded

SANDISK CORPORATION'S OPENING CLAIM CONSTRUCTION BRIEF
FOR THE SANDISK PATENTS

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SanDisk Corporation ("SanDisk") asserts that STMicroelectronics, N.V. and STMicroelectronics, Inc. (collectively, "ST") infringe claims 15 and 22 of U.S. Patent No. 5,583,812 ("the '812 patent") and claims 1-2, 4-21, and 23 of U.S. Patent No. 5,719,808 ("the '808 patent") (collectively, "SanDisk patents"). The parties have identified claim terms from the SanDisk patents for construction and have exchanged proposed constructions for those terms.[1] This claim construction brief explains SanDisk's proposed constructions for the terms identified. Each of SanDisk's proposed constructions is consistent with the understanding of persons of ordinary skill in the art of the '812 and '808 patents.

Because the proper construction requires an understanding of the technology of which the patents are a part, SanDisk provides herewith a technology tutorial[2] that generally explains the technology from which the SanDisk patents originate—flash memory technology—and generally explains the inventions described by the SanDisk patents.

I. LEGAL STANDARDS

Claim construction is a legal question for the court, which should first look to the intrinsic evidence comprising the claims, the specification, and the prosecution history.[3] Claim construction must begin with the words of the claim, which should be given their ordinary and customary meaning to a person of ordinary skill in the art at the time of the purported invention, *i.e.*, as of the effective filing date.[4] "Properly viewed, the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent."[5]

[1] For the Court's convenience, a table showing side-by-side comparisons of the parties' respective proposed claim constructions is attached as Exhibit 1.

[2] The technology tutorial is separately provided on a compact disk.

[3] *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315-17 (Fed. Cir. 2005); *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977-78 (Fed. Cir. 1995).

[4] *Phillips*, 415 F.3d at 1315.

[5] *Id.* at 1321.

In its *en banc Phillips* decision, the Federal Circuit avoided providing "a rigid algorithm for claim construction;" rather, the court identified the various sources of information the judge should review when construing a disputed term.[6] Those sources include:

- The claims themselves, and particularly the context in which a term is used within a claim, as well as the way the term is used in other claims of the patent;[7]
- The patent's specification, which the court reiterated is the primary basis for construing the claims;[8]
- The patent's prosecution history, which consists of the complete record of the proceedings before the Patent Office and includes the prior art cited during the examination of the patent;[9] and
- Extrinsic evidence, which consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries and learned treatises. The Federal Circuit has recognized that extrinsic evidence is especially helpful to a court to better understand the underlying technology and the way in which one of ordinary skill in the art might use the claim terms.[10]

In identifying these sources, the court recognized that "[b]ecause the meaning of a claim term as understood by persons of skill in the art is not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to 'those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean.'"[11] Thus, absent a clear redefinition or novel meaning identified by the inventor in the intrinsic evidence, the court is required to review these sources to identify the ordinary meaning of the claim term.[12]

While the Federal Circuit has provided a variety of directions regarding the claim construction process, it tempered strict reliance on sequences of analysis and types of evidence, recognizing that

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[6] *Id.* at 1324.

[7] *Id*. at 1314.

[8] *Id.* at 1315-16.

[9] *Id.* at 1317.

[10] *Id*. at 1317-19.

[11] *Id*. at 1314.

[12] *Id.* at 1324.

"there is no magic formula or catechism for conducting claim construction. . . . The sequence of steps used by the judge in consulting various sources is not important; what matters is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law."[13] Even so, the *Phillips* decision continues to recognize the validity of the court's observation in *Renishaw PLC v. Marposs Societa' Per Azioni*, that "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction."[14]

II. THE '812 PATENT

A. BACKGROUND OF THE '812 PATENT

The '812 patent issued on December 10, 1996, and relates to Electrically Erasable Programmable Read Only Memory (EEPROM) systems.[15] Generally, semiconductor memory systems, of which EEPROM systems are a part, utilize transistors to store or help store information in a memory cell. The memory cell typically stores binary information—a logic "1" or logic "0." According to typical conventions, a logical "1" occurs when the memory cell is charged or at a high voltage, while a logical "0" occurs when the memory cell is at a low voltage. While prior-art EEPROM systems generally were limited by the ability of each cell to be programmed to one of only two states—logic "1" or "0"—the '812 patent discloses a system and method in which the memory cells are individually capable of storing more than two states.[16] For example, in the preferred embodiment each memory cell can be programmed to any one of four distinct states: 0, 1, 2 or 3, which in turn represent two bits of binary information:

[13] *Id.* at 1324.

[14] 158 F.3d 1243, 1250 (Fed. Cir. 1998)

[15] The '812 patent also relates to Erasable Programmable Read Only Memory (EPROM), which is related to EEPROM. For the sake of simplicity, all references are made to EEPROM.

[16] *See generally* SanDisk's Technology Tutorial for the SanDisk Patents, filed concurrently herewith.

"00," "01," "10" or "11."[17] The ability of each cell to store more than one bit of information increases memory density and, in turn, reduces cost per unit of memory.

B. SANDISK'S PROPOSED CLAIM CONSTRUCTION OF THE '812 PATENT

SanDisk accuses ST of infringing claims 15 and 22 of the '812 patent. The following claim terms were identified by one or both parties for judicial construction. The parties dispute the meaning of each of the terms except the first term listed below.

1. "simultaneously comparing a resulting level of an electrical parameter of the addressed cell with a number of reference levels of two or more"

The parties agreed that this claim term, which is found in claim 15, means: "comparing a particular electrical response of an addressed cell with multiple distinct reference levels at the same time."[18]

2. "effective threshold voltage level"/"effective threshold voltage level of the addressed cell"

As explained in the '812 patent, the threshold voltage of a transistor is the voltage that must be applied to the gate of a transistor to turn the transistor on.[19] With respect to an electrically programmable read only memory (EPROM) cell, the '812 patent specifically explains that the memory transistor of such a cell has both a "control gate" and a "floating gate" and that the threshold voltage of the memory transistor is controlled by the amount of charge retained by the transistor's floating gate.[20]

In view of the specification, and the claim language, the proper construction of "effective threshold voltage level"/"effective threshold voltage level of the addressed cell" is:

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[17] *See, e.g.*, '812 patent, col. 4, ll. 38-50, attached as Exhibit 2.

[18] SanDisk agreed with ST's proposed construction of this term on February 15, 2006. At 5:00 p.m. on the day of filing, sT notified SanDisk that ST may not continue to propose its original construction, although ST gave no reason why it might change its proposed construction or what new construction ST might propose.

[19] *Id.* at col. 1, ll. 30-34 (The threshold voltage is "the minimum amount of voltage (threshold) that must be applied to the control gate before the transistor is turned 'on' to permit conduction between its source and drain regions . . ..").

minimum amount of voltage that must be applied to the control gate before the transistor is turned "on" to permit conduction between its source and drain regions; the minimum voltage results from a combination of a natural threshold voltage and a voltage responsive to a controllable level of charge on the floating gate, wherein said natural threshold voltage corresponds to that when the floating gate has a level of charge equal to zero

This claim term appears in claims 15 and 22 and is explicitly defined in claim 22 as:

> … said transistor having an effective threshold voltage resulting from a combination of a natural threshold voltage and a voltage responsive to a controllable level of charge on the floating gate, wherein said natural wherein said natural threshold voltage corresponds to that when the floating gate has a level of charge equal to zero

The language of claim 15 confirms that the definition in claim 22 also applies to claim 15.[21] Specifically, claim 15 states that the memory cell "has a threshold voltage level that is a given level in the absence of net charge on [its] floating gate but which is variable in accordance with an amount of net charge carried by said floating gate." In other words, the charge on the floating gate contributes to the "effective threshold voltage" of the transistor.

ST's proposed construction—"minimum amount of voltage that must be applied to the control gate before the transistor is turned 'on' to permit conduction between its source and drain regions"—partially borrows from a passage in the "Background of the Invention" section of the '812 specification,[22] but without completing the passage's explicit reference to the floating gate, *i.e.*, "is controlled by the level of charge on the floating gate."[23] ST's proposed construction, thus, erroneously ignores the explicit definition found in claim 22 as well as the full text of the patent specification. SanDisk's proposed construction is correct.

(continued…)

[20] *Id.* at col. 1, ll. 22-37; Fig. 1.

[21] *Phillips*, 415 F.3d at 1314 ("Because claim terms are normally used consistently throughout the patent, the useage of a term in one claim can often illuminate the meaning of the same term in other claims.").

[22] *See* '812 patent, col. 1, ll. 28-34.

3. "individually detectable states"

SanDisk contends this term, which appears in both claims 15 and 22, means:

states of a memory cell that can be identified from each other using electrical means

The idea of multiple, individually detectable states is central to the function of any memory cell. Indeed, any type of memory cell must have at least two individually detectable states corresponding to "on" or "off" and, in turn, a logical "1" or "0."[24] The '812 patent teaches and claims a system with more than two individually detectable states per memory cell such that each cell can store more than one bit of information. Claim 15, for example, states:

> Establishing a plurality of effective threshold voltage levels in excess of two that corresponds to a plurality of *individually detectable states* of the cell in excess of two,

In other words, and consistent with the understanding of effective threshold voltage explained above and the ordinary meaning of the words used, the claim describes a memory cell capable of storing more than two states. The written description is consistent:

> This invention proposes for the first time a scheme to take advantage of the full memory window. This is done by using the wider memory window to store more than two binary states and therefore more than a single bit per cell. For example, it is possible to store 4, rather than 2 states per cell, with these states having the following threshold voltage:
>
> State "3": V_{T1}=-3.0 V, V_{T2}=+1.0 V (highest conduction)=1, 1.
>
> State "2": V_{T1}=-0.5 V, V_{T2}=+1.0 V (intermediate conduction)=1, 0.
>
> State "1": V_{T1}=+2.0 V, V_{T2}=+1.0 V (lower conduction)=0, 1.
>
> State "0": V_{T1}=+4.5 V, V_{T2}=+1.0 V (no conduction)=0, 0.[25]

(continued…)

[23] *Id.* at col. 1, ll. 33-34.

[24] *See id.* at col. 1, ll. 38-44 (describing prior art one-bit-per-cell systems).

[25] *Id.* at col. 4, ll. 38-51.

The specification further teaches that the number of distinct states per memory cell is not limited to four.[26] It also teaches that measuring conduction is not the only possible method for distinguishing between states.[27]

ST proposes that "individually detectable states" means "conduction states of a memory cell that may be identified from each other using electrical means."[28] ST's proposed construction improperly limits the claim to the use of "***conduction*** states" for distinguishing storage states, which is contrary to the express teachings of the specification: "voltage level sensing rather than conduction level sensing can be employed."[29] ST's proposed construction should be rejected.

4. "electrically interrogating the addressed cell"

This term appears in claim 15 of the '812 patent and means:

applying appropriate voltages to the memory cell to measure the state of the cell

The context of the claim indicates that this claim term concerns "reading" the state of the memory cell:

> reading the state to which the addressed cell has been set by ***electrically interrogating the addressed cell*** and simultaneously comparing a resulting level of an electrical parameter of the addressed cell with a number of reference voltages of two or more.[30]

Specifically, an electric current is applied to the control gate of an addressed cell (electrical interrogation) to cause some level of current (including possibly no current) to flow between the cell's source and drain regions; that current (or lack of current) is then compared to reference current. Hence, the transistor can be "turned on" at variable levels by generating variable currents across the source and drain, and the memory interprets the logical value of the detected current by comparing it to reference voltages. This

[26] *Id.* at col. 4, ll. 52-65.

[27] *Id.* at col. 7, ll. 5-10.

[28] *See* Joint Claim Construction Statement at Exhibit G, p. 1 [Docket No. 55, filed Jan. 3, 2006].

[29] '812 patent at col. 7, ll. 8-10.

variable operation occurs, in part, by adjusting the effective threshold voltage through the charge on the floating gate.[31] Once the cell has been electrically interrogated, its output—"I_{DS}" in the preferred embodiment—is provided to one or more sense amplifiers that are capable of distinguishing the various states of the memory cell.[32]

ST's proposed construction—"placing appropriate voltages on an addressed cell's source, drain, and control gate and measuring the resultant electrical behavior of said cell"—improperly reads in limitations from the specification. Specifically, ST seeks to read in the patent's explanation of the prior art into its construction. For instance, the '812 patent explains that the general method used to interrogate memory cells in prior art, single-bit-per-cell systems:

> The memory cell transistor's state is read by ***placing an operating voltage across its source and drain and on its control gate***, and then detecting the level of current flowing between the source and drain as to whether the device is programmed to be "on" or "off" at the control gate voltage selected.[33]

While some cells may be interrogated in such a manner, *i.e.*, using the source, drain and control gate, neither the written description, nor the claim, require that those structures necessarily be used when interrogating a memory cell. Indeed, ST's construction completely omits how the charge on the floating gate affects how the memory cell operates. ST's construction should be rejected.

5. "base level"

This term appears in claim 22 of the '812 patent and means:

a threshold voltage from which programming (to a desired threshold voltage) can begin

The term "base level" is a part of the following means-plus-function clause:

(continued…)

[30] *Id.* at col. 11, ll. 63-67.

[31] *See, e.g.*, '812 at claim 22 ("altering the charge on the floating gate of an addressed cell until its effective threshold voltage is substantially equal to one of a plurality of threshold voltage levels in excess of two corresponding to a plurality of individual detectable states in excess of two").

[32] *Id.* at col. 4, ll. 52-59.

[33] *Id.* at col. 1, ll. 38-44.

> erasing means operably connected to said array for driving the effective threshold voltage of an addressed cell or group of cells to a ***base level*** by altering the charge on the floating gates of the individual addressed cell's floating gate[34]

The '812 patent explains that all memory cells are erased to a uniform "base level"—a predetermined threshold voltage—prior to programming the memory cells to a storage state. From that "base level," each cell can be programmed to a particular effective threshold voltage level corresponding to a desired storage state.[35]

ST contends that "base level" should be construed to mean "a threshold voltage more negative than the threshold voltage of the most conductive state of the memory cell." Once again, ST improperly attempts to read an example from the preferred embodiment into its construction.[36] SanDisk does not contest that one "***example***" provided by the preferred embodiment describes erasing "a voltage V_{T1} more negative than the '3' state . . .."[37] But, that is explicitly an example and, as such, cannot be used to limit the claim. Indeed, elsewhere in the specification the '812 patent provides other examples where a cell need not be erased to a threshold voltage more negative than the threshold voltage of the most conductive state. For instance, the inventor discusses erasing the device to a threshold voltage ***equal to*** the threshold voltage of the most conductive state of the memory cell (state "3" in the preferred embodiment).[38] Accordingly, the Court should reject ST's proposal and adopt SanDisk's construction of this term.

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[34] This means-plus-function term is addressed in Section II(C)(2), herein below.

[35] *See id.* at col. 5, ll. 18-35 ("First, it is required that the device be erased to a voltage V_{T1} more negative than the '3' state (-3.0V in this example). Then the device is programmed . . . to the desired one of four states (dashed lines in FIG. 2c).").

[36] *See, e.g., Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

[37] '812 patent, col. 5, ll. 21-23.

[38] *See id.* at col. 8, ll. 31-39 ("Assume that a block array of mxn memory cells is to be fully erased (Flash erase) to state '3' (highest conductivity at lowest V_{T1} state). Certain parameters are established in conjunction with the erase algorithm. They are listed in FIG. 3: V_1 is the erase voltage of the first erase pulse. V_1 is lower by perhaps 5 volts from the erase voltage required to erase a virgin device to state '3' in a one second erase pulse. t is chosen to be approximately $1/10^{th}$ of the time required to fully erase a virgin device to state '3'."). *See also id.* at Fig. 3 ("SET $I_{\text{"3"}}$ = CELL CONDUCTANCE IN FULLY ERASED STATE").

C. '812 PATENT CLAIM TERMS GOVERNED BY 35 U.S.C. § 112, ¶ 6

The parties agree that claim 22 of the '812 patent contains five means-plus-function terms governed by 35 U.S.C. § 112, ¶ 6. Means-plus-function limitations are construed in two steps. First, the Court must identify and construe the function of the claim element.[39] Second, the Court must identify structure in the patent that corresponds to the claimed function.[40]

1. "means operably connected to said array for addressing a selected one or group of the plurality of memory cells"

This claim limitation specifies addressing one or more memory cells as its function. The specification discloses the following structure that corresponds to this function:

word line decoder, bit line decoder

The preferred embodiment of the '812 patent is depicted in Figure 2e, which includes "Word Line Decode" and "Bit Line Decode" circuits. Referring to Figure 2e, the specification states, "In this circuit an array of memory cells has decoded word lines and decoded bit lines connected to the control gates and drains respectively of rows and columns of cells."[41] It further explains that the word line decoder and bit line decoder perform the function of addressing specific cells to be programmed or read.[42]

ST proposes that '812 patent discloses the following corresponding structure:

> word line connected to control gate of Flash memory cell, and controlled by the word line decode transistor, bit line connected to source of memory cell, and controlled by the bit line decode transistor, split channel cell[43]

ST's proposed construction is overly inclusive. First, ST contends that the cell itself is part of the structure that addresses the cell, *e.g.*, "control gate of Flash memory cell" and "source of memory cell."

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[39] *See Med. Instrumentation and Diagnostic Corp. v. Elekta AB*, 344 F.3d 1205, 1210 (Fed. Cir. 2003).

[40] *See id.* at 1211-12.

[41] '812 patent, col. 6, ll. 10-12.

[42] *Id.* at col. 1, ll. 44-49 ("A specific, single cell in a two-dimensional array of EPROM cells is ***addressed*** for reading by application of a source-drain voltage to source and drain lines in a column containing the cell being addressed, and application of a control gate voltage to the control gates in a row containing the cell being addressed."). *See also id.* at col. 6, ll. 28-43 ("A single short programming pulse is applied to both the selected word line and the selected bit line.").

The cell, of course, cannot address itself. ST contends, moreover, that the cell must be a "split channel cell." While the preferred embodiment describes a split channel cell, claim 22 is not so limited, and, in any event, the split channel cell does not address one or more memory cells—the function of this claim limitation. By its very specific proposal, ST seeks to confuse the need to identify structure corresponding to a claimed function with the prohibition against reading the preferred embodiment into the claim.[44] ST's proposed construction is further flawed by the inclusion of the word line and bit line. The word line and bit line merely carry current to/from the memory cell. It is the word line decoder and bit line decoder that actually determine which word line and bit line are activated so that particular cells are addressed.

Thus, as proposed by SanDisk, it is the word line decoder and bit line decoder that perform the function of addressing a selected one or group of the plurality of memory cells.

2. "erasing means operably connected to said array for driving the effective threshold voltage of an addressed cell or group of cells to a base level by altering the charge on the floating gates of the individual addressed cell's floating gate"

This limitation contains an obvious typographical error; namely, the end of the limitation should read ". . . altering the charge on the floating gates of the individual addressed ***cells***" and not "individual addressed cell's ***floating gate***." As the '812 patent makes clear, memory cells—not floating gates—are addressed.[45] The Court can correct this typographical error through claim construction. Indeed, the Federal Circuit has held that "[w]hen a harmless error in a patent is not subject to reasonable debate, it can be corrected by the court, as for other legal documents."[46]

(continued…)

[43] Joint Claim Construction Prehearing Statement at Exhibit G, pp. 2-3.

[44] *See, e.g., Acromed Corp. v. Sofamor Danek Group, Inc.*, 253 F.3d 1371, 1382-83 (Fed. Cir. 2001) ("Under 35 U.S.C. § 112, ¶ 6, a court may not import into the claim structural limitations from the written description that are unnecessary to perform the claimed function.").

[45] *See, e.g.*, '812 patent, col. 1, ll. 38-49; col. 6, ll. 9-28.

[46] *Hoffer v. Microsoft Corp.*, 405 F.3d 1326, 1331 (Fed. Cir. 2005).

With this obvious correction in place, this claim limitation recites the function of erasing a memory cell by altering the charge on its floating gate. The specification discloses that the following, corresponding structure executes this function:

erase electrode

This claim limitation refers to the means by which memory cells are erased to the base level.[47] Various methods for erasing EEROM cells were well known to persons of ordinary skill in the art.[48] In the "Description of the Preferred Embodiments" the specification discloses,

> The generic split-channel EPROM or EEPROM structure of FIG. 1 becomes a Flash EEPROM device when an erase gate 31 (FIG. 1a) is added. The erase gate is a separate electrode positioned near a portion of the floating gate 27 and separated from it by a tunnel dielectric 33. When the proper voltages are applied to the source, drain, substrate, control gate and erase gate, the amount of charge on the floating gate is reduced. A single erase gate extends to a large number of memory cells, if not the entire array, so that they may be erased all at once. In some prior art Flash EEPROM cells the source or drain diffusions underneath the floating gate are used also as the erase electrode, while in other cells the erase electrode is implemented either in the same conductive layer as the control gate or in a separate conductive layer.[49]

This passage thus identifies the existence of several structures in the art that may be used to erase memory cells to a base level. The '812 patent generically refers to these structures as "erase electrodes," and uses an erase gate as an exemplary erase electrode. Thus, the "erase electrode" is the structure that performs the function of driving the effective threshold voltage of an addressed cell to a base level.

ST asserts that the corresponding structure is composed of the following: "erase gate 31 and the proper voltages applied to the source, drain, substrate, control gate, and erase gate split channel cell."[50] ST's proposed construction is incorrect because, again, it is limited to the preferred embodiment and fails

[47] *See* Section II(B)(5) above (discussing "base level").

[48] Indeed, the second "E" in "EEPROM" stands for "Erasable."

[49] '812 patent, col. 3, ll. 47-61.

[50] Joint Claim Construction Prehearing Statement at Exhibit G, p. 3.

to reflect the inventors' express disclosure of erase electrodes other than an erase gate.[51] Furthermore, ST again tries to limit claim 22 to a "split channel cell." Claim 22's preamble, however, recites the structure required of a memory cell within the scope of claim 22. It does not require that the cell be split channel. Finally, ST's inclusion of "proper voltages …" is wrong because voltages are not structure.

3. "programming means operably connected to said array for altering the charge on the floating gate of an addressed cell until its said effective threshold voltage is substantially equal to one of a plurality of effective threshold voltage levels in excess of two corresponding to a plurality of individual detectable states in excess of two"

The function recited in this claim limitation is programming a memory cell by altering the charge on its floating gate. The specification discloses the following, corresponding structure for this element:

programming control circuit, word line program/read pulse generator, bit line program pulse generator

The '812 patent specification provides a concise description of how a four-state memory cell can be programmed at column 6, lines 28-43. In that passage, and referring to Fig. 2e, the structures directly corresponding to the function of programming the cell are the programming control circuit (activated when programming is required), word line program/read pulse generator, and bit line program pulse generator (both controlled by the programming control circuit).

ST contends that all of the following structures correspond to programming:

> [1] word line decode transistor, [2] word line, [3] word line program/read pulsing circuitry, [4] bit line precharge circuitry, [5] bit line, [6] bit line decode transistor, [7] bit line program pulsing circuitry, and [8] programming control circuitry, along with [9] voltages VPWL of ~12V and VPBL of ~9V, [10] sense amplifiers 0-3, [11] $I_{REFS\ 0\text{-}3}$, [12] split channel cell.[52]

Buried in ST's litany of proposed corresponding structures are the three structures identified by SanDisk. As noted above, the Federal Circuit in its *Acromed* decision corrected a court's attempt to limit a 112 ¶ 6

[51] *TI Group Automotive Systems, Inc. v. VDO North America, L.L.C.*, 375 F.3d 1126, 1137 (Fed. Cir. 2004) ("[w]hen multiple embodiments in the specification correspond to the claimed function, proper application of § 112, [paragraph 6] reads the claim element to embrace each of those embodiments."), *quoting, Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

[52] Joint Claim Construction Prehearing Statement at Exhibit G, pp. 4-5.

element to specifics found in the preferred embodiment that are unnecessary to perform the recited function.[53] The other structures (and voltages) proposed by ST, however, are not necessary for performing the claimed function of "altering the charge on the floating gate of an addressed cell":

- The word line and bit line, which ST seeks to include, simply carry the signals generated by the word line program/read pulse generator and bit line program pulse generator—they do not perform the recited function.

- The word line decode transistor and bit line decode transistor, which, as explained above in Section II(C)(1), perform the claimed addressing function—not the programming function—and thus are structure corresponding to the addressing means, not the programming means.

- The bit line precharge circuitry is not a part of the claimed programming means. Rather, the bit line program pulse generator identified by SanDisk generates the signal that is applied to the bit line during programming.

- "Voltages VPWL of ~12V and VPBL of ~9V" are not structure. These specific voltages, like the specific dimensions rejected by the Federal Circuit in *Acromed*, are unnecessary to perform the claimed function.

- Sense amplifiers constitute the "determining means" and "comparing means" (*see* Sections II(C)(4), (5) below) and are not part of the programming means.[54] Sense amplifiers are not directly involved in programming.

- $I_{REF\ 0\text{-}3}$ are not structures, rather they are reference currents produced by the "plurality of reference sources" recited in a separate limitation of claim 22.[55]

- ST's attempt to limit the programming means to a split channel cell is wrong. First, the memory cell is what is programmed, so it is not a part of the structure used to program. Next, nothing in the description of Fig. 2e references a split channel transistor. Indeed, Fig. 2e generically refers to a "flash EEPROM cell," not to a split channel cell.

[53] 253 F.3d 1382-83 ("To limit the body portion to a diameter at least as large as the crest diameter of the second externally threaded portion would be to impermissibly import into the claim limitation specific dimensions of a preferred embodiment that are unnecessary to perform the claimed function of blocking effluence and restricting transverse movement. This court will not limit a patent to its preferred embodiments in the face of evidence of broader coverage by the claims."). *See also, Micro Chem.*, 194 F.3d at 1258 ("[T]he statute [does not] permit incorporation of structure from the written description beyond that necessary to perform the claimed function.").

[54] *See* 812 patent, col. 6, ll. 28-43 (explaining role of sense amplifiers in determining whether to apply programming pulses).

[55] *See id.* at col. 13, ll. 20-21 ("a plurality of reference sources providing a number of different reference current levels of two or more").

SanDisk has correctly identified the three structures responsible for programming a memory cell by altering the charge on its floating gate: the programming control circuit, word line program/read pulse generator and bit line program pulse generator.

4. "means operably connected to said array for determining the amount of current that flows through an addressed cell"

Analogous to claim 15's "electrically interrogating the addressed cell," the function associated by this limitation concerns reading the current flowing through an addressed cell. The specification discloses the following, corresponding structure for this limitation:

sense amplifiers

The written description discloses: "To sense any one of these four states, the control gate is raised to V_{CG}=+5.0 V and the source-drain current I_{DS} is sensed through the composite device."[56] The resulting source-drain current, I_{DS}, is then provided to sense amplifiers, which are capable of determining the amount of current flowing between the source and drain regions.[57] Thus, it is the sense amplifiers, which are connected to the array, as illustrated in Fig. 2e, that determine the amount of current that flows through an addressed cell.[58]

As it has with the limitations discussed above, ST seeks to include structures that go beyond those necessary to perform the identified function:[59] ST identifies the following structures:

> word line, word line decode transistor, word line program/read pulsing circuits, bit line, bit line precharge circuits, bit line decode transistor, split channel cell.[60]

[56] *Id.* at col. 4, ll. 52-54.

[57] *Id.* at col. 4, ll. 58-59.

[58] The use of sense amplifiers to determine the amount of current flowing through an addressed cell was known throughout the field. *See, e.g.,* Ashok K. Sharma, SEMICONDUCTOR MEMORIES: TECHNOLOGY, TESTING, AND RELIABILITY, 124 (IEEE Press 1997) ("In an erased cell, the select-gate voltage is sufficient to overcome the transistor turn-on threshold voltage (V_T), and the drain-to-source (I_{DS}) current detected by the sense amplifier produces a logic '1.'"), attached as Exhibit 3.

[59] In hopes of reaching agreement regarding the construction of this limitation, SanDisk proposed a compromise that included the word line program/read pulsing circuit. Indeed, this structures does "turn on" the control gate of the memory cells such that current can flow through an addressed cell, provided the charge on the floating gate permits the flow of any current. It is, however, the sense amplifiers that determine the amount of current, if any, that flows through the cells once the control gate has been turned on.

[60] Joint Claim Construction Prehearing Statement at Exhibit G, p. 4.

The word line decode transistor and bit line decode transistor are the means that address a memory cell (*see* Section II(C)(1), above) and are not involved in determining the current that flows through an addressed cell. Neither does the bit line precharge circuit determine the current that flows through an addressed cell.[61] Additionally, as explained above, the word line and bit line simply carry signals; they do not perform the function of determining the amount of any such signal. Finally, for the reasons also explained above ST's attempt to include a "split channel cell" is in error.

5. "means including a number of sense amplifiers of two or more for simultaneously comparing the amount of current flowing in an addressed cell with said number of reference current levels, whereby the state of an addressed cell is rapidly read"

This means-plus-function limitation recites the function of determining the state of a memory cell. This function equates to claim 15's "simultaneously comparing a resulting level of an electrical parameter of the addressed cell with a number of reference levels of two or more," described above. The specification discloses the following, corresponding structures that perform this function:

plurality of sense amplifiers, plurality of reference current sources

The written description teaches that, when reading a memory cell, the cell's current output is supplied to a plurality of sense amplifiers for comparison against a plurality of reference current levels. Indeed, Figure 2e discloses four sense amplifiers with each having an input from the bit line carrying I_{DS} from the memory cell being read and an input from one of four references ($I_{REF,\,0}$, $I_{REF,\,1}$, $I_{REF,\,2}$, $I_{REF,\,3}$). Each sense amplifier individually compares the amount of current flowing in an addressed cell with the reference current level supplied to it from its respective reference current source. The simultaneous comparisons made by the plurality of sense amplifiers yield the state of the addressed cell. Referring, for example, to Figure 2e, the written description provides,

> For a four state storage, four sense amplifiers, each with its own distinct current reference levels $I_{REF,\,0}$, $I_{REF,\,1}$, $I_{REF,\,2}$, and $I_{REF,\,3}$ are attached to each decoded

[61] *See, e.g.*, '812 patent, col. 6, ll. 14-16 ("Each bit line is normally precharged to a voltage between 1.0V and 2.0V during the time between read, program or erase.").

> output of the bit line. During read, the current through the Flash EEPROM transistor is compared simultaneously (i.e., in parallel) with these four reference levels ….[62]

Thus, the sense amplifier reads the state of an addressed cell, and using the reference current sources "is capable of easily distinguishing between these four conduction states."[63]

ST contends that the structures corresponding to this means-plus-function limitation are "sense amplifiers 0-3, reference currents I_{REF0-3}, buffers D0-D3, split channel cell."[64] ST again seeks to overload the construction:

- While ST correctly includes sense amplifiers, it incorrectly attempts to limit the structure to ***four*** sense amplifiers, "0-3." The claim, however, consistent with the '812 specification, [65] is not so limited and specifically recites "a ***number*** of sense amplifiers ***of two or more*** …"

- While the sources of the reference currents constitute structure, the currents themselves, *i.e.*, "reference currents I_{REF0-3}," are not. And, as with the sense amplifiers, neither the reference current sources nor the currents themselves are limited in number. [66] Indeed, because the '812 patent clearly explains that the number of storage states is variable, so too are the number of structures that provide those states. [67]

- ST also incorrectly seeks to include the four "buffers D0-D3." But, the claimed function merely describes "simultaneously comparing the amount of current flowing in an addressed cell with said number of reference current levels." Buffers D0-D3 simply receive and store the ***output*** from their respective sense amplifiers and have no role in the recited function.

- Finally, for all of the reasons explained above ST's effort to limit the claim to "split channel cells" must be rejected. Indeed, the cell, split channel or otherwise, cannot be a part of the structure because it is the cell's output current that the claim requires be compared to the reference current levels.

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[62] *Id.* at col. 6, ll. 16-25.

[63] *Id.* at col. 4, ll. 58-59; *see generally id.* at col. 4, ll. 38-65 (sense amplifiers distinguish between the multiple possible states of a memory cell). *See also id.* at col. 5, ll. 28-32 ("The device is then sensed by comparing its conduction current I_{DS} with that of a reference current source I_{REF}, i (i=0, 1, 2, 3) corresponding to the desired conduction state …."). *See also id.* at col. 7, ll. 5-10 (warning against limiting the invention to the circuitry depicted in Figure 2e).

[64] Joint Claim Construction Prehearing Statement at Exhibit G, p. 4.

[65] '812 patent, col. 6, ll. 58-66 ("In actual fact, although four reference levels and four sense amplifiers are used to program the cell into one of four distinct conduction states, only three sense amplifiers and three reference levels are required to sense the correct one of four stored states.").

[66] *See id.* at col. 4, ll. 59-65 (more than four states per cell possible).

[67] *Id.*

SanDisk has properly identified the structures associated with each claimed function, and respectfully requests that the Court adopt SanDisk's proposed constructions for the '812 patent.

III. THE '808 PATENT

A. BACKGROUND OF THE '808 PATENT

The '808 patent relates to an inventive system and architecture for performing erase in a Flash Electrically Erasable Programmable Read Only Memory (EEPROM) system.[68] Flash memory systems permit a user to repeatedly write (store) information in a memory cell and read (retrieve) that information from the cell. When data stored by a memory cell is no longer needed, that memory cell must first be erased before new data can be placed in that cell.[69] As the '808 patent explains, prior-art systems adopted a rigid approach to erasing memory cells. Some prior-art systems erased an entire chip at one time. Other prior-art systems erased one sector at a time. The prior-art systems did not have the flexibility to adjust or optimize the size of erasure to the specific performance needs of the flash memory system. The "one size fits all" prior-art approach to flash memory erase operations was inefficient and time-consuming.[70]

The '808 patent discloses and claims a system that sectored flash memory (where all cells within a sector are erasable together), where each sector can be separately selected and addressed for erasure, and where a combination of sectors can be selected and addressed for erasure with a single command.[71] To facilitate this technique, the '808 system uses logic circuitry located on the flash memory chip, and distinct from the controller chip,[72] to manage the erasure of selected sectors. Not only is multi-sector

[68] *See generally* SanDisk's Technology Tutorial for the SanDisk Patents.

[69] '808 patent, col. 4, ll. 25-32, attached as Exhibit 4.

[70] *Id.* at col. 4, ll. 33-50.

[71] *Id.* at col. 4, ll. 51-57.

[72] The controller communicates data and instructions to the flash memory array. *See, e.g., id.* at col. 3, ll. 31-33 (Fig. 1A) and col. 3, ll. 58-63 (Fig 1B).

erasure faster than prior art schemes, but it requires less involvement by the controller, thereby freeing up the controller to tend to other tasks during erasure.

B. SANDISK'S PROPOSED CLAIM CONSTRUCTION OF THE '808 PATENT

SanDisk accuses ST of infringing claims 1, 2, 4-21, and 23 of the '808 patent. The following claim terms were identified by one or both parties for judicial construction.

1. "sectors that individually contain a plurality of said cells … which are erasable together" / "the cells of the individual sectors being erasable together"

The first of these related claim terms appears in '808 claims 1, 16 and 23, while the latter appears in claims 5 and 11. The following construction should apply to both terms:

all of the cells within a given sector are erased as a group

As noted above, the '808 patent teaches dividing the memory cell arrays into a functional group of cells called "sectors."[73] The patent also explains that erasing a sector causes all of the sector's cells to be erased "at once" or "together," *i.e.*, as a group.[74] Given this context, and the plain claim language, the Court should construe the phrases simply as "all of the cells within a given sector are erased as a group."

ST contends that the claim term means, "sectors that individually contain a plurality of cells … which are erasable as a group at substantially the same time." ST seeks to confuse and limit the plain meaning of the claim language by injecting a temporal component—"at substantially the same time"—to the definition. Nothing in the '808 patent, however, requires erasing "together" as meaning "at substantially the same time." Instead, the cells in a sector are erased together (as a group) using a single command, as the preferred embodiment of '808 patent exemplifies.[75] By contrast, in a related patent that

[73] *Id.* at col. 1, ll. 61-63 ("According to one aspect of the present invention, an array of Flash EEprom cells on a chip is organized into sectors such that all cells within each sector are erasable at once."); col. 4, ll. 51-53 ("In the present invention, the Flash EEprom memory is divided into sectors where all cells within each sector are erasable together.").

[74] *Id.*

[75] *Id.* at col. 5, ll. 43-48 ("After all sectors intended for erase have been selected, the controller then issues to the circuit 220, as well as all other chips in the system a global erase command in line 251 along with the high voltage for erasing in line 209. The device will then erase all the sectors that have been selected (i.e. the sectors 211 and 213) at one time.").

shares the same specification as the '808 patent, the inventors expressly included a temporal limitation in the claims: "… an array of Flash EEprom cells partitioned into a plurality of sectors, each sector addressable for erase such that all cells therein are ***erasable simultaneously*** …."[76] Thus, given the way in which the '808 patent describes the invention, as well as the plain language of the claims, the Court should reject ST's construction that erroneously attempts to inject an "extraneous" time element into the construction.[77]

2. "subjecting the EEPROM cells . . . in parallel to erase voltages"

This term appears in '808 claim 1 and has means:

providing a voltage suitable to erase the cells in the selected sectors simultaneously

Unlike the previous claim terms, which used the non-technical word "together," the use of the word "parallel" in this phrase does denote to one of skill in the art simultaneous action. This is supported by reference to definitions of "parallel" in technical dictionaries:

> [ELEC] Connected to the same pair of terminals. Also, known as multiple; shunt.[78]
>
> *Electricity*. A side-by-side connection in which the same voltage is applied to all components.[79]

Because the EEPROM cells are electrically connected in "parallel," *i.e.,* connected to the same terminals and thus subjected to the same erase voltage, the cells are erased simultaneously. The '808 patent, moreover, explains that "erase voltages" are voltages of sufficient strength and duration to cause erasure

[76] U.S. Patent No. 5,418,752 at claim 1, attached as Exhibit 5.

[77] *See, e.g., E.I. Du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988) ("By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim. "). Here, nothing in the '808 specification even suggests a temporal limitation is required.

[78] *McGraw-Hill Dictionary of Scientific and Technical Terms* 1366 (4th ed. McGraw-Hill 1989), including Figure of "Parallel Circuit," attached as Exhibit 6.

[79] *Dictionary of Science and Technology* 1570 (Academic Press 1992), attached as Exhibit 7.

of all the memory cells in a sector.[80] SanDisk's construction comports with the understanding of those skilled in the art and the context provided by the '808 patent.

ST contends that this claim term means "applying, at substantially the same time, multiple appropriately high voltage levels to cause erasure of the selected EEPROM cells."[81] By inclusion of the word "multiple voltage levels" in its construction, ST again impermissibly attempts to read the preferred embodiment into the claim. While the '808 patent does provide an example where voltage line (Ve) is raised to a specified value for a specified duration, and that step is repeated if erasure is not verified,[82] that is simply the way in which the preferred embodiment operates; as a matter of law, that specific operation cannot be read into the construction.[83] Furthermore, ST's recognition that "parallel" adds a temporal component evidences the error of ST's construction of "together." The redundancy that arises from ST's constructions makes no sense in the context of the claims or '808 specification. ST's proposal should be rejected in favor of SanDisk's construction.

3. "erase together all the enabled sectors"

This term appears in claims 5 and 11 and means:

erase all of the selected sectors as a group in response to a single erase initiation command from the controller

One of the central ideas of the '808 patent is the ability of the controller to issue a single erase command to the flash memory chips to initiate the erasure of a selected combination of sectors. This is supported by the '808 specification, which, as explained above, teaches using a single "global erase

[80] '808 patent, col. 6, ll. 20-28.

[81] Joint Claim Construction Prehearing Statement at Exhibit H, p. 1.

[82] *See, e.g.,* '808 patent, col. 6, ll. 24-31.

[83] *Phillips*, 415 F.3d at 1323 ("[A]though the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments. … In particular, we have expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.").

command" to erase all selected sectors,[84] as opposed to the "prior art schemes where all the sectors must be erased every time or only one sector at a time can be erased."[85] The one-sector-at-a-time approach required the controller it issue erase commands for each sector. The requirement that a controller issue multiple commands to erase multiple sectors as opposed to a single erase command undermined system performance. In contrast, when a controller uses only a single initiate erase command, system performance is enhanced because the controller is free to perform other tasks during the erase operation.[86] SanDisk's construction captures this objective of the invention and is the correct construction.[87]

ST's proposed construction—"erase as a group at substantially the same time all sectors that have been selected for erasure"—while capturing the concept of a group, again seeks to inject a temporal limitation where none exists. Neither the '808 specification nor the claims require the multiple sectors be erased "at substantially the same time." Indeed, as explained above, where the inventors desired simultaneity they used that word[88] or a similar word, *e.g.*, "parallel." This point is further evidenced by the fact that in claim 9, which depends from claim 5, requires erasure of "all the enabled sectors in parallel," *i.e.*, simultaneously. Construing claim 5 to the same scope as claim 9, runs afoul of the requirements for dependent claims under 35 U.S.C. § 112, ¶ 4 and the doctrine of claim differentiation.[89] Thus, by using the term "together" in claims 5 and 11, instead of "simultaneously" or "parallel," the inventors elected a broader scope for the instant claim term. Consistent with Federal Circuit authority,

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[84] '808 patent, col. 5, ll. 43-48.

[85] *Id.* at col. 1, l. 67 – col. 2, l. 3. *See also id.* at col. 4, ll. 33-50 (distinguishing two exemplar prior art systems).

[86] *See id.* at col. 7, ll. 7-13 (controller free to perform read and write operations while erasure is ongoing).

[87] *Phillips*, 415 F.3d at 1316 ("Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim."), *quoting, Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998).

[88] *See* U.S. Patent No. 5,418,752 at claim 1 ("means for ***simultaneously*** performing the erase operation on only the plurality of selected sectors.") (emphasis added), attached as Exhibit 5.

[89] 35 U.S.C. § 112, ¶ 4 "[A] claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed." *See also Dow Chem. Co. v. United States*, 226 F.3d 1334, 1341 (Fed. Cir. 2000) ("The doctrine of claim differentiation … creates a rebuttable presumption that each claim in a patent has a

SanDisk has captured the inventors' intent and correctly construed "together," which appears in multiple claims, consistently as referring to a group.[90]

4. "erase . . . sectors in parallel"

This claim term appears in dependent claims 9, 15, and 21 and means:

simultaneously provide a voltage to all of the selected sectors; said voltage being suitable to erase the cells in the selected sectors simultaneously

As explained above, by using the term "in parallel," the inventors intended erasure of the selected sectors to occur simultaneously. Figure 3A shows parallel connection of the sectors and, given the understanding that one of ordinary skill in the art would have regarding parallel circuits, it is clear that the inventors contemplated simultaneous erasure.[91]

ST proposes that, for claims 9 and 15, the claim term means "erase as a group at substantially the same time all sectors that have been selected for erasure" and, for claim 21, it means "erase as a group at substantially the same time the combination of sectors that have been selected for erasure."[92] ST's construction of these dependent claims is identical to its construction of the phrase "erasing together all the enabled sectors" appearing in independent claim 5. [93] This overlapping construction violates the rule of claim differentiation and the purpose of independent and dependent claims, further illustrating the error of ST's constructions.

(continued…)

different scope."); *Phillips*, 415 F.3d at 1314-15 ("[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.").

[90] *See, e.g., Phillips*, 415 F.3d at 1314 ("claim terms are normally used consistently throughout the patent").

[91] *See also* '808 patent, col. 5, ll. 48-51.

[92] Joint Claim Construction and Prehearing Statement at Exhibit H, pp. 3-4.

[93] The slight change in ST's proposed construction for claim 21 does not diminish this point.

5. "register associated with individual ones of the sectors to tag its respective sector as enabled for erasure"

This term appears in claim 6 and means:

an information storage circuit containing information denoting whether an associated sector(s) is selected for erasure

In order to permit a plurality of, but less than all, sectors for erasure, the memory system requires some way to identify the sectors selected for erasure. The preferred embodiment described in the '808 patent uses registers to identify which sectors have been selected for erasure:

> FIG. 3A illustrates a block diagram circuit 220 on a Flash EEprom chip (such as the chip 201 of FIG. 2) with which one or more sectors such as 211, 213 are selected (or deselected) for erase. Essentially, each sector such as 211, 213 is selected or tagged by setting the state of an erase enable register such as 221, 223 associated with the respective sectors.[94]

Claim 6 simply reflects this aspect of the preferred embodiment, which SanDisk's proposed construction recognizes.

ST's proposed construction—"register associated in one-to-one correspondence with an individual sector in memory to uniquely identify its associated sector as enabled for erasure"—rewrites the limitation to include a "one-to-one correspondence" between register and sector. No such requirement appears in either the claim or the '808 patent specification. In fact, during prosecution of the '808 patent, the Examiner was put on notice that a on-to-one correspondence was not required.[95] Indeed, as quoted above, and captured in SanDisk's construction, the specification simply describes an "association" between registers and respective sectors.

[94] '808 patent, col. 5, ll. 9-15.

[95] *See* Prosecution History for U.S. Patent App. Serial No. 08/407,916 ('808 patent); Request for Continuance of Prosecution, Attachment (Initial Determination) at 44-46 (Apr. 23, 1997), attached as Exhibit 8. In prior litigation in the International Trade Commission involving the '752 patent, which shares the same specification as the '808 patent, the presiding administrative law judge rejected this argument when construing the claim language "individual register associated with each sector for holding a status to indicate whether the sector is selected or not." The ALJ found: "[T]here is not indication in the claim language or specification that the claimed invention is restricted to the preferred method of constructing registers and arranging them in an exclusive, one-to-one correspondence with the sectors." *Id.*

6. "plurality of registers that individually contain a tag indicating whether an associated sector is enabled for erasure or not"

This term appears in claim 12 and means:

information storage circuits each containing information denoting whether an associated sector(s) is selected for erasure

This claim term is almost identical to the previous term, except that this term calls for a "plurality of registers." The terms convey the same idea and should be construed similarly.[96]

As with the previous claim term, ST's proposed construction—"plurality of registers in one-to-one correspondence with individual sectors in memory that contain information indicating whether that associated sector is enabled for erasure or not"—attempts improperly to rewrite the claim to include a "one-to-one correspondence" between register and sector. For the reasons given above, including "one-to-one correspondence" in the construction should be rejected.

7. "setting a tag bit"

This term appears in claims 18 and 19 and means:

setting a bit in a register to indicate that the sector(s) associated with the register is selected for erasure

The claim essentially defines this term: "wherein designating the combination of sectors includes ***setting a tag bit*** for individual ones of the sectors to be erased . . . ." Thus, the term identifies the mechanism by which the memory system enables a sector for erase. The claim language is consistent with the specification, which teaches that sectors selected for erasure are "tagged by setting the state of an erase enable register . . . ."[97]

ST's proposed construction—"setting the appropriate erase enable register to a HIGH value"—improperly limits this claim term to the preferred embodiment by requiring that an erase enable register

[96] *Phillips*, 415 F.3d at 1314.

[97] '808 patent, col. 5, ll. 12-15.

be set to HIGH. While the preferred embodiment operates in this manner, such a scheme is arbitrary, and the claims are not so limited. To do so would violate the rule against reading limitations from the specification into the claims.

8. "clearing the tags"/"clearing tags"/"clearing the tag bits"

These nearly identical terms appear in claims 1, 7, 13 and 19 and mean:

resetting the bits in registers so that the registers no longer indicate that the respective sector(s) associated with each register is selected for erasure

Once sectors selected for erasure have been erased, the tag bits that denote the sector should be erased are cleared from the respective registers associated with the erased sectors. This is clear from the claim language itself: ". . . ***clearing tags*** from those registers of a particular combination of sectors which are verified to be erased . . . ."[98] By clearing the tag bit corresponding to a particular sector(s), the system indicates that erasure is no longer needed for that sector(s). The specification provides a more detailed description of this activity at column 6, lines 14-42.

ST's proposed construction—"resetting the appropriate erase enable registers to a LOW value"—improperly copies the details of the preferred embodiment into the construction. While the '808 patent discloses a preferred embodiment in which an erase enable register is switched to LOW ("0") once erasure has occurred,[99] that embodiment is merely illustrative. There is nothing in the claims, specification or prosecution history that requires a "LOW value" to clear a register; to do so would violate the Federal Circuit's mandate against reading examples into the claim. ST's proposal should be rejected.

[98] *Id.* at claim 7, col. 16, ll. 44-46.

[99] *Id.* at col. 6, ll. 31-36.

9. "maintaining an identification of those of said multiple sectors that are defective"

This term is found in claims 2 and 20 and means:

storing the identities of sectors that do not operate properly

Despite the clear language of the claims, ST has asked that this phrase be construed. SanDisk has done so using the plain meaning of the words in the claims and consistent with the context of the '808 patent, which describes various ways in of identifying defective sectors in the memory system.[100]

ST's proposed construction—"maintaining a map in memory that identifies defective sectors"—is wrong because it seeks to limit the claim to mapping in memory. While the '808 patent discusses memory mapping in the context of identifying defective sectors it does so only in the context of its preferred embodiment. ST's blatant attempt to read, yet again, the preferred embodiment into the claims should be rejected.

10. "a logic circuit configured to address and enable for erasure, in response to signals from the controller, any combination of a plurality of but less than all of said multiple sectors"

This term appears in claim 5 and means:

a logic circuit on a memory chip that is responsive to signals from a controller and can enable for erasure any combination of sectors from the set of permissible sector-erase combinations; each combination must consist of at least two but less than all sectors

This claim term identifies one of the central ideas of the '808 patent—a memory system that performs multiple-sector erase by issuing a single global erase initiation command from a controller to a logic circuit on the memory chip that implements erasure of the selected combination of sectors. As explained in above, prior art systems allowed for erasure of the entire chip at once or erasure of one sector at a time. Through Figure 1B, and reference to certain prior art systems, the '808 patent explains that requiring the controller (shown as 31 in Figs. 1A and 1B) to issue repeated commands to each sector selected for erasure is time consuming. The '808 patent avoids this inefficiency by enabling multiple

sectors to be erased with one command from the controller, [101] but executed by logic on the memory chips, which frees the controller in the system to access other memory chips and do read and write operations on them.[102]

Circuit 220 of Figure 3A provides an illustration of a logic circuit configured to address and enable erasure of a combination of sectors.[103] As explained in the '808 patent, the controller (via lines 209) provides the addresses of selected sectors for erasure.[104] The logic circuit 220 of the flash memory chip contains decoders and registers that enable erasure of multiple selected sectors.[105] When the global erase initiation command is provided to the flash memory chip, the logic circuit causes the selected sectors to be erased as a group.[106]

The '808 patent, and SanDisk's construction, moreover, recognizes that the combination of sectors selected for erasure must come from those sectors capable of being erased. Indeed, the patent identifies a significant advantage in being able to skip sectors, such as defective or unused sectors, [107] and to flexibly configure sectors to be erased to save power. [108] SanDisk's construction takes into account each of these components of the invention.

ST offers the following proposed construction:

(continued…)

[100] *See, e.g., id.* at col. 2, ll. 28-29 ("Another feature of the invention allows defect mapping at the sector level."); *id.* at col. 11, ll. 31-58 (describing various methods for defective mapping, *i.e.*, storing the identities of defective sectors).

[101] *Id.* at col. 5, ll. 43-48 (describing "global erase command").

[102] *Id.* at col. 7, ll. 8-11.

[103] *Id.* at col. 5, ll. 9-51.

[104] *Id.* at col. 4, ll. 58-61; *id.* at col. 5, ll. 17-24.

[105] *Id.* at col. 5, ll. 18-24.

[106] *Id.* at col. 5, ll. 43-51.

[107] *Id.* at col. 6, ll. 43-55 ("Additional advantage is that if a sector is ***bad*** or is ***not used*** for some reason, that sector can be skipped over with now erase occurring within that sector.") (Emphasis added).

[108] *See id.* at col. 6, ll. 56-65 ("The flexibility in erase configuration of the present invention enables the adaptation of the erase needs to the power capability of the system.").

> a circuit configured to send address information and appropriate erase enable signals to enable selection and erasure of any combination of more than one but less than all (excluding selection of one and excluding selection of all) of the addressable sectors in the memory in response to signals from the controller[109]

Buried in ST's proposed construction is the notion that the logic circuit must be able to select ***any*** combination of sectors on the memory chip(s), ignoring the patent's teaching that unused or defective sectors can be skipped. Nothing in claim 5, the '808 patent specification or prosecution history limits the invention to a system necessarily capable of selecting any and every conceivable combination of sectors. ST's proposed construction should be rejected.

11. "a logic circuit configured to enable erasure of any one of multiple different combinations of a plurality of but less than all of said multiple sectors"

This claim term appears in claim 11, and, similar to the preceding limitation, means:

a logic circuit on a memory chip that is responsive to signals from a controller and can enable for erasure at least two different combinations of sectors; each combination must consist of at least two but less than all sectors

This term is analogous to the previously discussed term from claim 5 except that it does not explicitly require that the logic circuit be configured to ***address*** the combination of sectors. Given this similarity, this term should be construed consistently with the previous claim term, yet reflecting the slightly broader scope of the instant term. ST apparently agrees with this point given the similarity in the constructions it proposed for these two terms.

ST offers the following proposed construction:

> a circuit configured to issue appropriate erase enable signals to enable the erasure of any one of the multiple different possible combinations of more than one but less than all (excluding selection of one and excluding selection of all) of the addressable sectors in the memory[110]

Because ST recognizes the similarity between the limitation of claim 5 and this limitation in claim 11, its proposed construction reflects the same error as that found in its claim 5 proposal: ST adds the notion

[109] Joint Claim Construction and Prehearing Statement at Exhibit H, p. 2.

that the logic circuit must be capable of enabling each and every conceivable combination of sectors for erasure. As explained, this notion conflicts with the disclosure of the '808 patent and should be rejected.

12. "combinations"

SanDisk contends this term has the following meaning:

Claim 16: Both instances of "combinations" (elements (a) and (d)) are typographical errors and should read "combination." Claim 23: The first instance of "combinations" in element (a) is a typographical error and should read "combination," but the second instance in element (a) is correct.

ST's insistence that the Court construe the everyday word "combinations" is unwarranted. ST's desire to construe these words is an attempt to inject ambiguity as a result of obvious typographical errors. Indeed, it is unnecessary to refer to anything other than the claims themselves understand that the claims contain *de minimis* typographical errors. Those claims recite,

> 16. A method . . . comprising:
>
> (a) designating ***a combinations*** of a plurality of but less than all of said multiple sectors to be erased,
>
> (b) erasing ***the combination*** of sectors without erasing others of said multiple sectors,
>
> (c) after ***the combination*** of sectors has been erased, writing data in at least some of the erased combination of sectors, and
>
> (d) repeating the operations of (a) through (c) with ***another combinations*** of sectors.
>
> * * * *
>
> 23. A method . . . comprising:
>
> (a) designating ***a combinations of any one of multiple different combinations*** of a plurality of but less than all of said multiple sectors to be erased,
>
> (b) erasing ***the combination*** of sectors without erasing others of said multiple sectors, and
>
> (c) after ***the combination*** of sectors has been erased, writing data in at least some of ***the*** erased ***combination*** of sectors.

(continued…)

[110] Joint Claim Construction and Prehearing Statement at Exhibit H, p. 4.

Of the four instances where "combinations" appears in claims 16 and 23, above, the first three instances—16(a), 16(d), and the first instance in 23(a)—are obvious typographical errors. The fourth instance—the second instance of "combinations" in 23(a)—is correct. Simply reading the terms in the context of the claims makes the typos readily apparent, *e.g.*, "***a*** combinations." As the Federal Circuit explained in *Hoffer*,[111] such obvious typographical errors can be corrected by the court during claim construction, and the Court should do so here.

IV. CONCLUSION

Based on the foregoing, SanDisk respectfully requests that the Court adopt SanDisk's proposed constructions.

[111] *Hoffer*, 405 F.3d at 1331.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies the foregoing document was filed electronically on February 21, 2006, pursuant to Local Rule CV-5(a) and has been served on all counsel who have consented to electronic service and on all other counsel by regular mail.

/s/Steven M. Geiszler
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